FPGA BASED GENERIC RADAR DISPLAY TRAINING SIMULATOR (RDTS)

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Abstract

FPGA (Field Programmable Gate Array) based generic display was developed and installed at NAVAL Shipyard Kochi for use by INDIAN NAVY as part of the Radar Display Training. The RDTS is used to facilitate testing /operator's training using various types of Naval Radar Displays like Color Tactical Display (CTD), MM950 Display, RAWL MK III VEXT (Video Extractor and Tracker), and Indigenous RAWL MK II Display etc. The RDTS generates various input signals required to test and provide operator's training for Naval Radar Displays. This paper presents the system overview, generation of simulated Radar input signals (Video, Sync, Azimuth and Heading line) in various formats (pulse/Synchro etc), generation of simulated ship's speed and heading information in pulse/Synchro format.

1 INTRODUCTION

This paper discusses the development of a FPGA based Generic Radar Display Training Simulator that has been designed to provide shore based Radar Display operator instruction for training functions that previously could only be carried out with Radar at factory. The simulator provides the ability to generate radar input signals such as surface targets, air targets, fixed targets, ship's speed and heading. It provides more flexibility, reliable and enables effective training. In this RDTS, multiple logical circuits are implemented by using FPGA, which

largely simplifies the design and improves the flexibility.

II SYSTEM OVERVIEW

Radar Display Training Simulator Unit (RDTS) is used for testing various types of Radar Displays like Color Tactical Display, MM950 etc. It generates the user selectable Video, PRF, Heading Line (HL), Azimuth (AZ) Pulses for simulating targets on the Radar Displays either through selection of parameters using local panel (or) programmable through a serial port interface. It generates the simulated SYNCHRO LOG, GYRO and AZ pulses for ship's speed information, ship's heading information etc. It can also generate around 200 simulated targets (Moving Target video, Fixed Target Video). Some of the target parameters (Range, Bearing, and Speed etc) are programmable through a serial port interface.

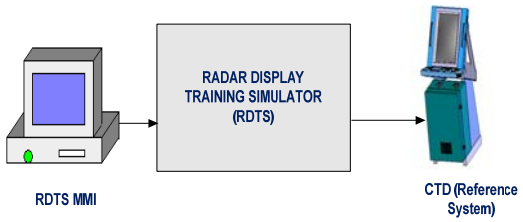

Figure: 1 Test Setup of RDTS

III DETAILED USER REQUIREMENT

The development began with detailed discussions about the subject matter with experts, the radar instructors. The requirements for a useful training tool were identified as

- Comprehensive, user friendly radar display training simulator (RDTS)
- Provision of local controls for On/Off, Video Intensity, Sync Pulse or Pulse Repetition Time (PRT) selection, heading line selection, Bearing pulse selection , No. of Targets selection etc.

  a) Selectable Heading line rate (3 to 50 r.p.m.).
  b) Selectable Azimuth pulses and Azimuth Synchro (90 to 8192).

c) Selectable Sync or Pulse Repetition Frequency (PRF) (250Hz to 4 KHz).
d) Selectable Synchro GYRO Fixed, Clockwise (CW) and Counter Clockwise (CCW).
e) Selectable LOG pulses (100, 200 Pulses/Knots) and Log Synchro (0 to 50 Knots).

- RDTS status monitoring panel

IV SYSTEM DESIGN

Fig 2 shows the system level schematic of the design. The heart of the Radar Simulator card is a FPGA that can perform most of the functions of the card. The FPGA selected is Cyclone II EP2C20F484.It is optimized for low cost applications including a wide range of density, memory, embedded multiplier, and packaging options**.** The interfaces of FPGA with other modules of the system are shown. The design includes interface with local control switches (i.e. Video selection switch, Sync/PRF selection switch, AZ or bearing selection switch, Heading selection switch, synchro selection switch etc). The user selected local control parameters will be read by the FPGA and written in to the input registers accordingly. The design also includes interface with MMI (Man machine Interface) through serial port. The RDTS MMI sends the commands to FPGA to generate user selected Video, Sync, AZ, HL and LOG outputs. The FPGA is interfaced with Digital to SYNCHRO Converter (DSC) to generate 90V L-L GYRO/LOG/AZ Synchro output. The RDTS status parameters will be displayed on the LCD panel or on the RDTS MMI.

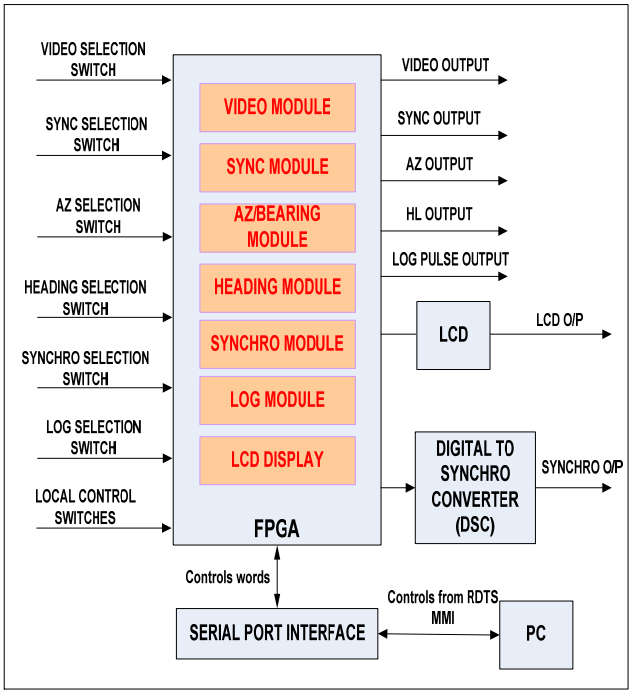

Figure: 2 System Level Block Diagram of Design

The total design is implemented on a single FPGA chip and the implementation solution utilizes the resource of FPGA (Type Cyclone-II series) so as to meet the user requirement.

1 *RDTS Features*

Features/Functions of the RDTS unit are listed below.

1) Generates user selectable Video, PRF or Sync, Heading Line (HL), Azimuth (AZ) or Bearing Pulses for simulating targets on the Radar Displays either through selection of parameters using hardware (or) programmable through an optional serial port interface.
2) Can generate around 200 simulated targets (Moving Target video, Fixed Target Video, Patch Video, Ring or circle Video) to test the display tracking function.
3) Various Target parameters(like Range, Bearing, Speed etc) are programmable through an Optional serial port interface using a (Personnel Computer) PC
4) Generates the simulated ships speed (LOG), heading (GYRO) in pulse/synchro formats
5) Provides a comprehensive test set up to provide operator training in shore based establishments without a need to connect to operating radar.

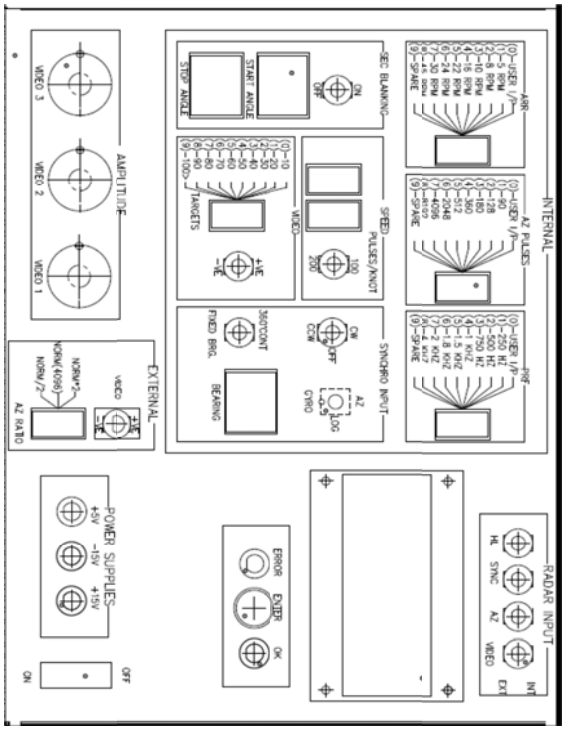

FIGURE 3: RDTS Local Panel/Control

V RADAR SIGNALS GENERATION

S.No.	Signals	Selection Type/Ranges
1	Video	+Ve (5V to 11V) / -Ve (-5V to –11V)
2	SYNC (Hz)	250, 500, 750, 1K, 1.5K, 1.8K, 2K, 4K +Ve (5V to 11V) or user programmable
3	HL (RPM)	5,8,10,16,22,24,30,45 +Ve (5V to 11V) or user programmable
4	AZ (No. of Pulses) or AZ SYNCHRO	90,128,180,360,512,2048,4096,8192 +Ve (5V to 11V) or user programmable
5	GYRO SYNCHRO	0 to 360 deg (90 V L-L)
6	LOG SYNCHRO And LOG Pulses	0 to 48 (Knots) (90 V L-L) 100 / 200 Pulses

Table 1: RDTS Signal Types

1 ***PRT/SYNC Generation***

The Pulse Repetition Frequency (PRF) of the radar system is the number of pulses that are transmitted per second. The time between the beginning of one pulse and the start of the next pulse is called pulse-repetition time (PRT) and is equal to the reciprocal of PRF as follows:

$$PRT = \frac{1}{PRF}$$

a) RDTS generates standard PRFs like (250Hz, 500Hz, 1 KHz, 2 KHz, 4 KHz), with different voltage levels (both TTL and upto 12V, with link settings) and it provides multiple outputs.
b) Different PRFs are selectable through local control switches.
c) RDTS generates Programmable PRFs (250 Hz -10 KHz PRF).

The RDTS reads the user selected PRF value and generates the PRT by using simple counters. For a radar set having a PRF of 1800 Hz and the corresponding PRT will be 555.55 micro sec. The RDTS generates the 555.55 micro sec SYNC or PRT of pulse width 1 micro sec.

2 ***VIDEO Generation***

The radar system pulse repetition frequency determines its ability to unambiguously measure target range. In order to obtain an unambiguous measurement of target range, the interval between radar pulses must be greater than the time required for a single pulse to propagate to a target at a given range and back. The maximum unambiguous range is then given by

$$R_{unamb.} = \frac{c_0}{2 \cdot PRF} = \frac{c_0 \cdot PRT}{2}$$

Where c_0 is the velocity of electromagnetic propagation = speed of light = $3 * 10^8$ m/s.

The distance is determined from the running time of the high-frequency transmitted signal and the propagation **c_0. Range** is the distance from the radar site to the target measured along the line of sight.

a) RDTS generates video with different voltage levels (settable through POT) and each one provides multiple outputs. It generates both positive and negative Video.

b) RDTS generates more than 200 targets (Patch video, Stationary targets and Moving target Video) and no. of targets can be selected through a switch.

The RDTS reads the user selected number of targets value and generates the video by using simple counters. For a radar set having a PRF of 1800 Hz, the maximum unambiguous range is given by

$$R_{unamb.} = \frac{c_0 * PRT}{2} = \frac{3*10^8 *555.55 * 10^{-6}}{2} = 83.333Km$$

3 ***ACP (Antenna Count/Change Pulse) Generation***

The angular determination of the target is determined by the directive of the antenna. The angular accuracy of the target is depends on the no. of ACP's.

a) RDTS generates standard ACPs like (8192, 4096, 2048, 1024, 512, 360, 180, 90), with different voltage levels (both TTL and up to 12V, with link settings) and it provides multiple outputs.
b) Different ACP's are selectable through local control switches and it also generates Programmable ACP's (1 RPM -90 RPM).
c) RDTS also generates synchro AZ (1:360) output.

The RDTS reads the user selected No. of ACP value and generates the ACP by using counters.

The RDTS generates the ACP pulses with 50% duty cycle and it also generates SYNCHRO Azimuth. The simulated digital angle values are distributed to 14 bit Digital to Synchro Converters (DSC). Then the RDTS generates the final 90 V L-L synchro output.

4 ***ARR (Antenna Rotation Rate) Simulation***

The more slowly the antenna rotates, the greater is the detection range of the radar.
For a radar set having a ACP of 4096 pulses and an antenna rotation rate of 6 RPM (1 revolution in 10 seconds or 36 scanning degrees per second), there is 1 pulse transmitted
each 0.087° of rotation.
The RDTS generates the 10 sec ARR of pulse width > 2 m sec.
Then,

$$\text{One ACP} = \frac{\text{ARR}}{\text{No. Of ACP pulses}} = \frac{10}{4096} = 0.00244 \text{ sec}$$

5 ***Ship's heading (GYRO) Simulation***

The RDTS generates two types of GYRO simulation (in Synchro format) outputs

a) FIXED BEARING

b) CONTINOUS (360deg/min)

a) FIXED BEARING: RDTS reads the selection for synchro gyro and fixed bearing values from local control panel for generating digital values in FPGA. The simulated digital values are distributed to 14 bit digital to synchro converter DSC. Then the RDTS generates the final 90 V L-L synchro output.

b) CONTINOUS (360deg/min): RDTS reads selection for continuous simulation from the local panel for generating continuous clockwise (CW) or anti-clockwise digital values in FPGA. The simulated digital values are distributed to digital to synchro converter (DSC). Then the RDTS generates the final 90 V L-L synchro output.

6 ***LOG (Ship's speed) simulation (SYNCHRO FORMAT AND PULSE)***

RDTS generates two types of LOG outputs

1). SYNCHRO LOG

2). PULSE LOG

1) SYNCHRO LOG: RDTS reads the selection for synchro log and Log values from local control panel for generating digital values (speed in knots) in FPGA.The simulated digital values are distributed to 14 bit digital to synchro converter (DSC). Then the RDTS generates the final 90 V L-L synchro output.

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2) PULSE LOG RDTS reads the selection for log pulses and Log values from local control panel for generating LOG pulses in FPGA. It generates 100/200 pulses output types.

FIGURE 4: Simulated Moving Targets

CONCLUSION:

Radar and sensor output signals have been simulated for testing various Radar Displays. Some of these features may be useful especially at shore or site, where complex Radar setup is not available and it can be used for operators training also. RDTS is very compact and cost effective system for evaluating Radar displays.

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REFERENCES:

[1] Skolnic : Radar Handbook
[2] Radar Design Principles Mc Graw-Hill, Inc.

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